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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,224	02/26/2002	James J. O'Brien	2001.042/1109.009	4797

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EXAMINER	
TABONE JR, JOHN J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/083,224	O'BRIEN ET AL.
	Examiner	Art Unit
	John J. Tabone, Jr.	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02262002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-75 have been examined.

Drawings

2. The drawings are objected to because descriptive labels other than numerical are needed for figure 7A. See 37 CFR 1.84(o). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

3. The examiner would like to point out that method claims are typically illustrated by a simple flowchart(s) with the boxes containing the steps of the method. These drawings aid in the understanding of the claimed invention.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-29 and 35-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bock et al. (US-5434804), hereinafter Bock.

Claims 1-29 and 35-75:

Bock teaches a JTAG test control device 18 (controller) and an In Circuit Emulator (ICE) test monitor 19 (emulator) are connected to chips 14 and 16 (a JTAG scan chain including multiple devices) of Printed Circuit Board (PCB) 12. Bock teaches the JTAG test control device 18 (controller) generates and processes test, debug and monitoring signals, for input and output to chips 14 and 16 (a JTAG scan chain including multiple devices) along conventional JTAG signal lines, namely, input (TDI)/output (TDO) (serial input/output ports), status (TMS), reset (JRESET) and clock line (JCLK). Bock also teaches the input and JTAG clock signals are transmitted from JTAG controller 26 to various JTAG registers (instruction register, idcode register, bypass register, data register, of claims 18-27, 50 –59, 67-70, 75) positioned within the microprocessor chip illustrated by JTAG registers, 28 and 29. Bock further teaches ICE monitor 19 (emulator) provides test signals, also along the conventional JTAG lines, for testing, monitoring or debugging internal functionality and interconnections of chip 14 (scan chain and TAP controller signal handler) through the JTAG pins are not be limited solely to JTAG test signals, but may include additional signals for testing the internal operation of chip 14 via an ICE within the chip (non-JTAG signal handler). Bock even further teaches at least some of the conventional ICE test pins may be retained on chips 14 and 16 to facilitate certain conventional ICE operations such as ICE commands for suspending operation of the chip (interrupt signal per claim 17). (Col. 4, lines 3-68, col.

5, lines 1-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made that systems, which include emulators and TAP controllers for the purpose of debugging multiple devices are commonly known in the art. The artisan would have been motivated to do so because these commonly know systems include all the limitations disclosed in independent claims 1, 26, 59, 66, 74 and 75 such as instruction and data memory structures, control logic coupled to the instruction and data memory structures as well as signal logic. Also, the artisan would have been motivated to do so because TAP controllers, which are commonly known in the art, include serial input port and said serial output port that are selectively coupled to one of the instruction memory structure and the data memory structure.

5. Claims 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bock et al. (US-5434804), hereinafter Bock, in view of Chung (US-6446230), hereinafter Chung.

Claims 30–34:

Bock does not explicitly teach the device can be implemented as a soft core or FPGA. However, Chung teaches a second embodiment of the invention using a second enabler 750 (device of controller), which works in conjunction with a TAP emulator 780 and provides boundary scan testability to a "TAP-less" DUT 742. TAP-less DUT 742 can be, for example, an in-system configurable (ISC) field programmable gate array (FPGA) or other type of programmable device (soft core) that does not have an internal TAP controller. (Col. 8, lines 47-52, FIG. 8A). It would have been obvious to one of

ordinary skill in the art at the time the invention was made to modify Bock's JTAG test control device 18 (controller) to works in conjunction with Chung's enabler 750 (device of controller). The artisan would have been motivated to do so because it would enable Bock's JTAG test control device 18 (controller) to be loaded into the soft cores via the scan chain.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Deao et al. (US-6055649)

Deao teaches JTAG controller and an emulator with much detail given to the opcodes, control states, etc. (Claims 1-29 and 35-75).

b. Bhattacharya (US-6381717)

Bhattacharya teaches JTAG controller and an emulator. (Claims 1, 26, 59, 66, 74, 75).

c. Deao et al. (US-6775793)

Deao teaches JTAG controller and an emulator. (Claims 1, 26, 59, 66, 74, 75).

d. Battaline et al. (US-5768152)

Battaline teaches JTAG controller and an in-circuit emulator ICE. (Claims 1, 26, 59, 66, 74, 75).

e. Brannick et al. (US-6289300)

Brannick teaches an embedded emulator. (Claims 46, 66, 74, 75).

f. Satoh (US-2001/00100083)

Satoh teaches a TAP controller and an in-circuit emulator ICE. (Claims 1, 26, 59, 66, 74, 75).

g. Whetsel (US-6408413)

Whetsel teaches a IEEE 1149.1 compliant TAP controller. (Claims 26, 70, 75).

h. Whetsel (US-2002/0002691)

Whetsel teaches a serial scan architecture that provides improved processor emulation capability. (Claims 46, 66, 74, 75).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (703) 305-8915. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John J. Tabone, Jr.
Examiner
Art Unit 2133

GUY J. LAMARRE
PRIMARY EXAMINER